LESSONPLAN

| Department:CSE | | Semester:3 rd ,NameofFaculty: |
|------------------------|-------------|--|
| Subject: | | Effective From Date: |
| Computer | No.of days/ | |
| System | week Class | No. of Week-15 |
| Architecture | allotted: 4 | |
| (CSA) | | TopictobeCovered: |
| Week | ClassDay | Theory |
| 1st | 1st | UNIT1:BASICSTRUCTUREOFCOMPUTER HARDWARE |
| | 2nd | 1.1 Basic Structure of computer hardware |
| | 3rd | 1.2FunctionalUnits |
| | 4th | 1.3Computercomponents |
| 2 nd | 1st | 1.4Performancemeasures |
| | 2nd | 1.5Memoryaddressing&Operations |
| | | 1. DoubtClearingclass |
| | 3rd | 2. Quiz test |
| | | 3. Assignment |
| | 4th | UNIT2:INSTRUCTIONS&INSTRUCTIONSEQUENCING |
| 3 rd | 1st | 2.1 Fundamental stoin structions |
| | 2nd | 2.2Operands |
| | 3rd | 2.3OP Codes |
| | 4th | 2.4Instructionformats |
| 4 th | 1st | 2.5AddressingModes |
| | | 1. DoubtClearingclass |
| | 2nd | 2. Quiz test |
| | | 3. Assignment |
| | 3rd | UNIT3:PROCESSORSYSTEM |
| | 4th | 3.1 RegisterFiles |
| 5 th | 1st | 3.2 Completeinstruction execution |
| | | ● Fetch |
| | 130 | • Decode |
| | | Execution |
| | 2nd | 3.3Hardwarecontrol |
| | 3rd | 3.4Micro programcontrol |
| | | 1. DoubtClearingclass |
| | 4th | 2. Quiz test |
| | | 3. Assignment |
| 6 th | 1st | UNIT4:MEMORY SYSTEM |
| | 2nd | 4.1Memory characteristics |
| | 3rd | 4.2Memory hierarchy |
| | 4th | 4.3RAMandROM organization |
| 7 th | 1st | 4.4Interleaved Memory |
| | 2nd | 4.5Cachememory |
| | 3rd | 4.6Virtualmemory |
| | | 1. DoubtClearingclass |
| | 4th | 2. Quiz test |
| | | 3. Assignment |

| 8 th | 1st | UNIT 5:INPUT-OUTPUT SYSTEM |
|------------------|-----|--|
| | 2nd | 5.1Input-OutputInterface |
| | 3rd | 5.2Modesof Data transfer |
| | 4th | 5.3 Programmed I/O Transfer |
| 9 th | 1st | 5.4InterruptdrivenI/O |
| | 2nd | 5.5 DMA |
| | 3rd | 5.6I/O Processor |
| | | 1. DoubtClearingclass |
| | 4th | 2. Quiz test |
| | | 3. Assignment |
| | 1st | UNIT 6:I/O INTERFACE&BUS ARCHITECTURE |
| | 2nd | 6.1 BusandSystemBus |
| | | 6.2 TypesofSystemBus |
| 10 th | 3rd | • Data |
| | | • Address |
| | | Control |
| | 4th | BUS |
| | 1st | 6.3 BusStructure |
| 11 th | 2nd | 6.4 Basic ParametersofBusdesign |
| | 3rd | 6.5 SCSI |
| | 4th | 6.6 USB |
| | 1st | 1. DoubtClearingclass |
| | | 2. Quiz test |
| 12 th | | 3. Assignment |
| 12 | 2nd | UNIT7:PARALLELPROCESSING |
| | 3rd | 7.1ParallelProcessing |
| | 4th | 7.2LinearPipeline |
| 13 th | 1st | 7.3Multiprocessor |
| | 2nd | 7.4Flynn"s Classification |
| | 3rd | Flynn "s Classification Types |
| | 4th | • SISD |

Signature of Faculty

Lecture , CSE ASIAN SCHOOL OF TECHNOLOGY, KHORDHA